

Fig. 1

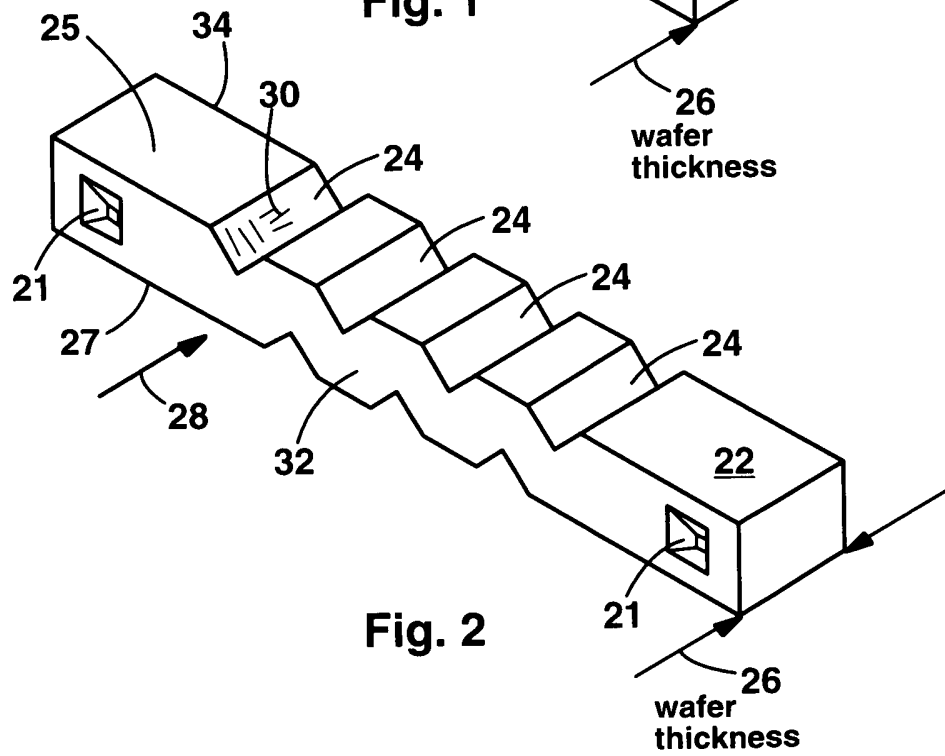
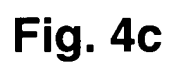
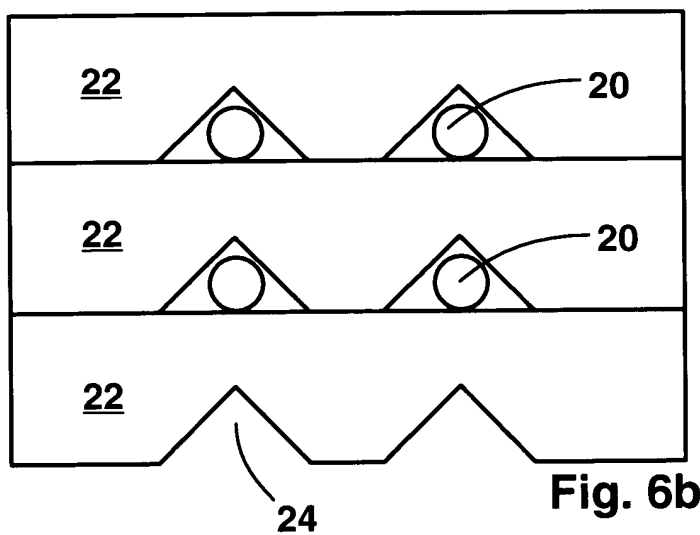
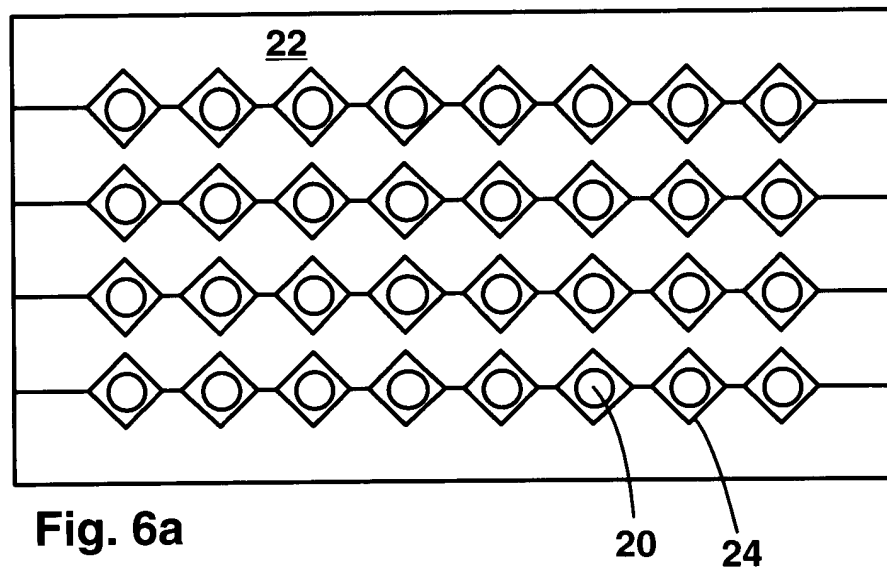
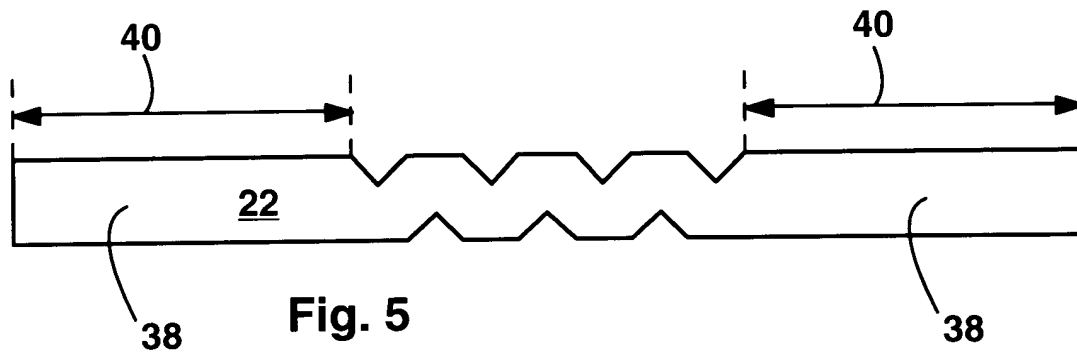


Fig. 2





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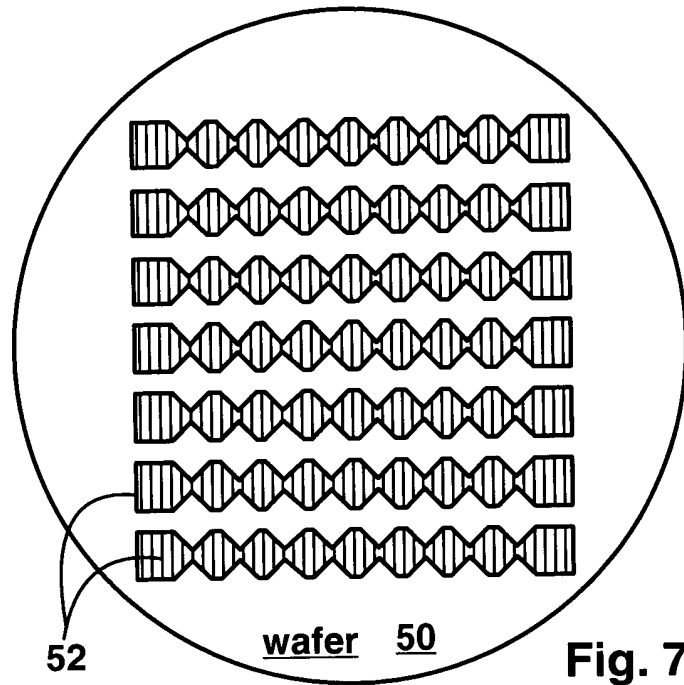


Fig. 7

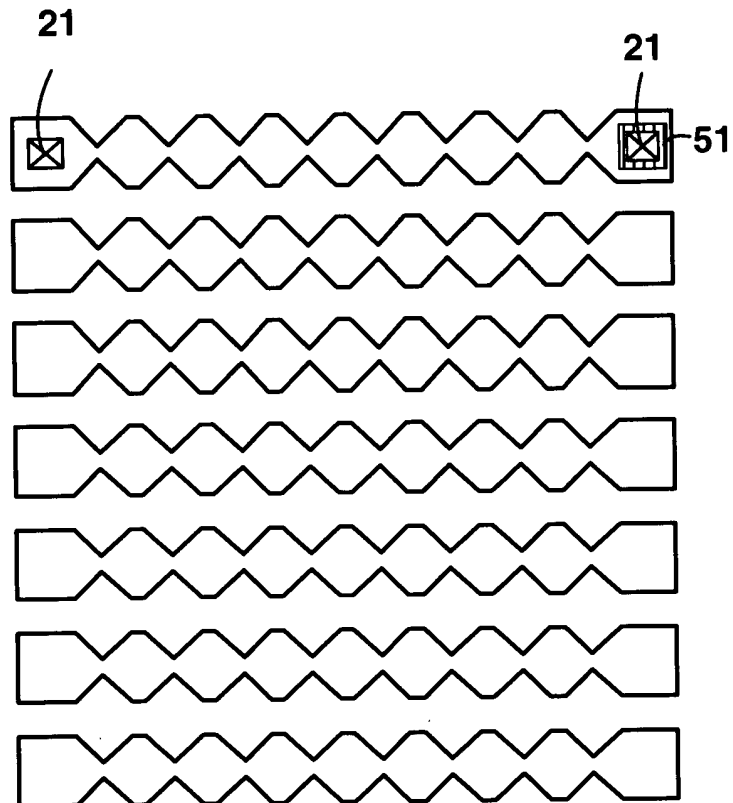
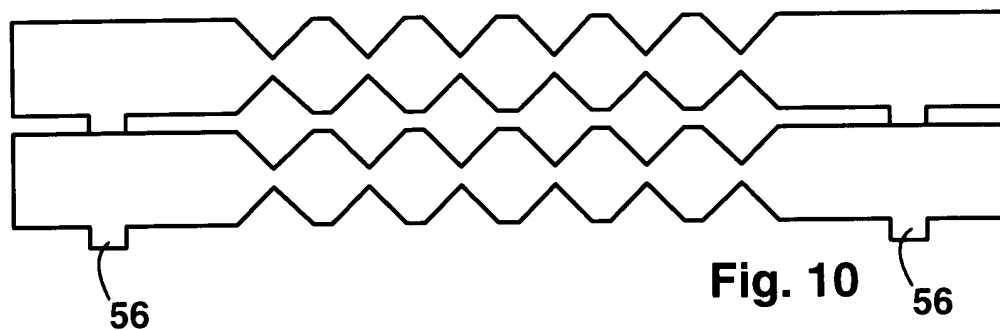
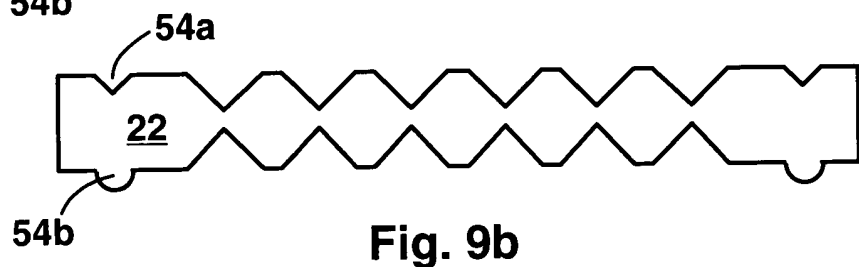


Fig. 8



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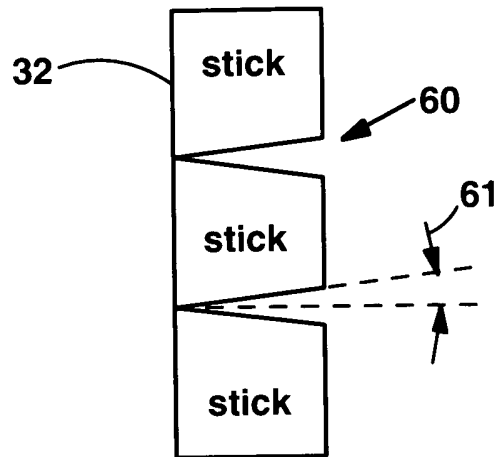


Fig. 12

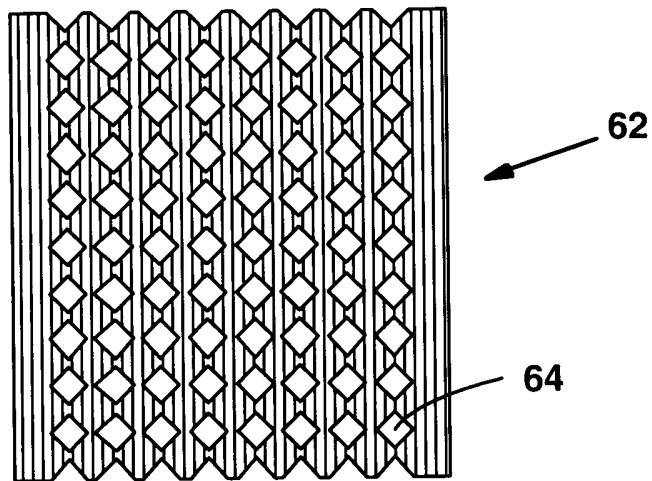


Fig. 13a

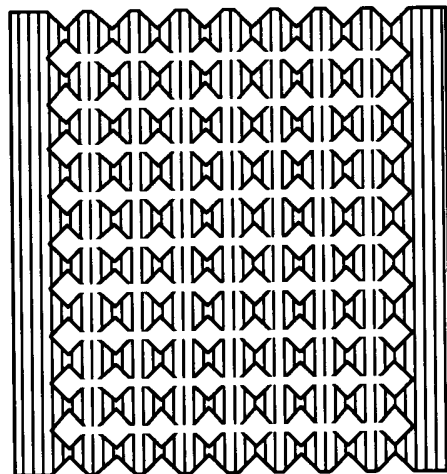
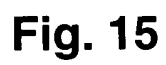
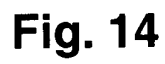
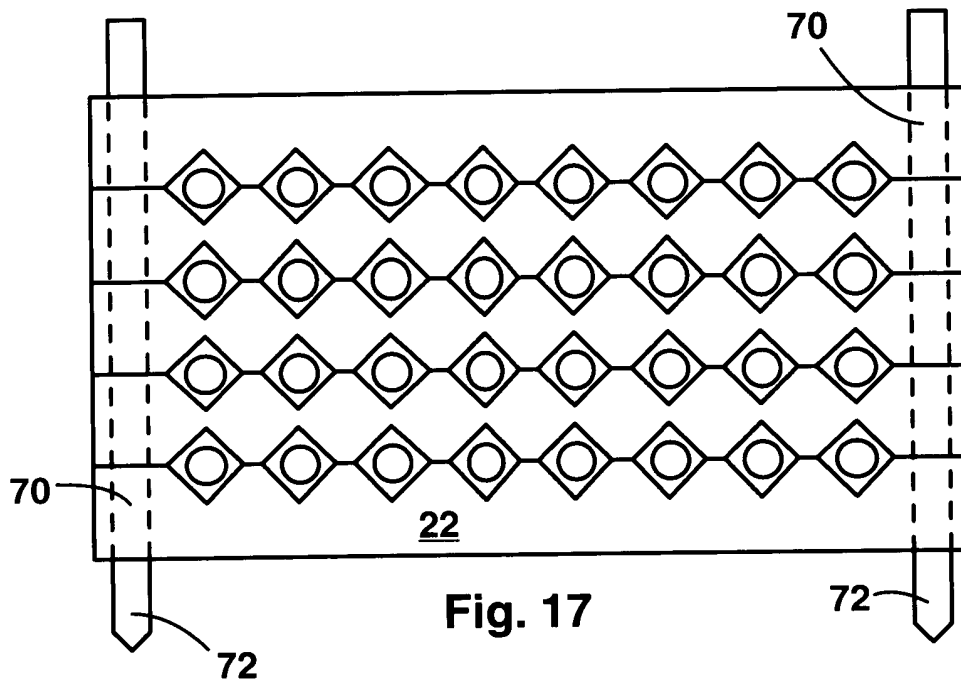
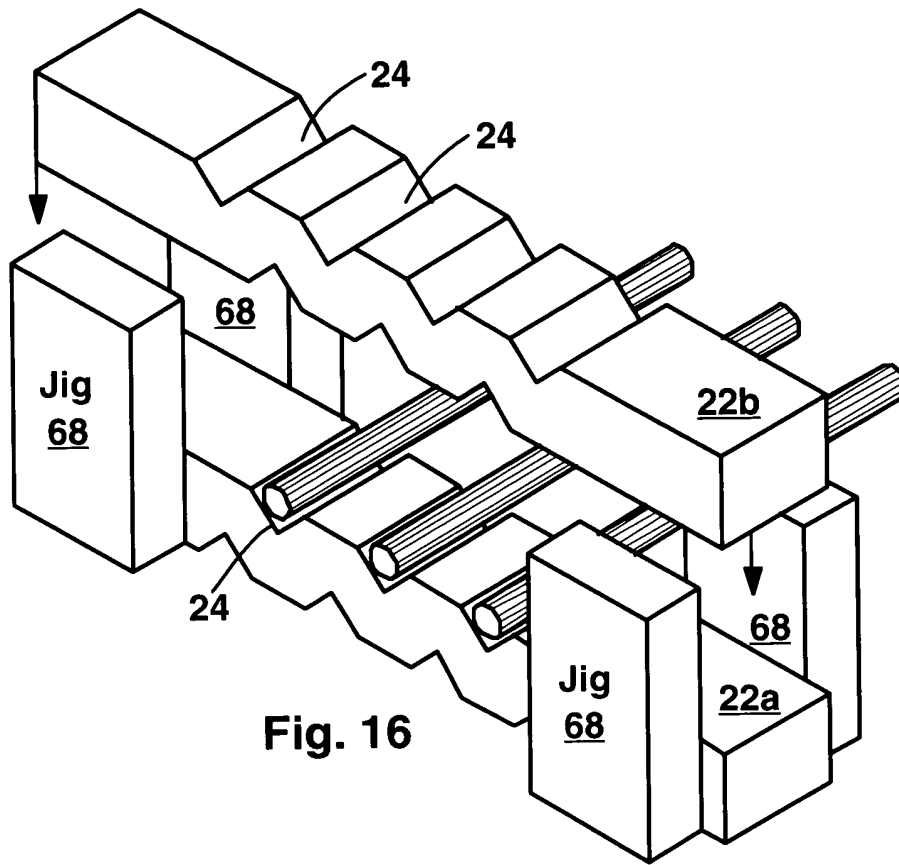


Fig. 13b

00ET20" TOTST960

**06-1070**







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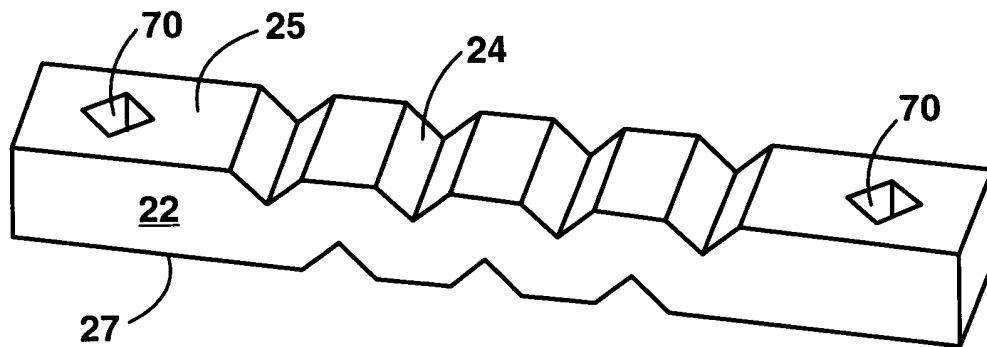


Fig. 18

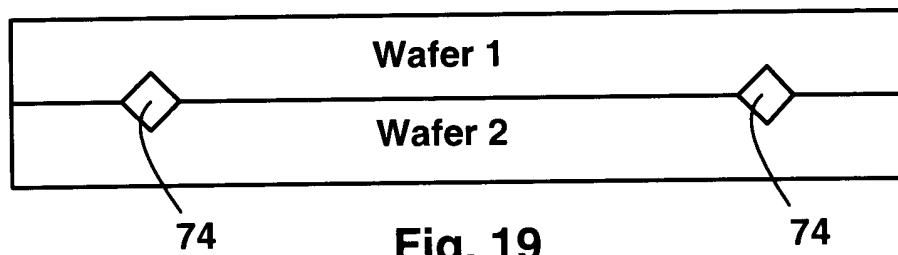


Fig. 19

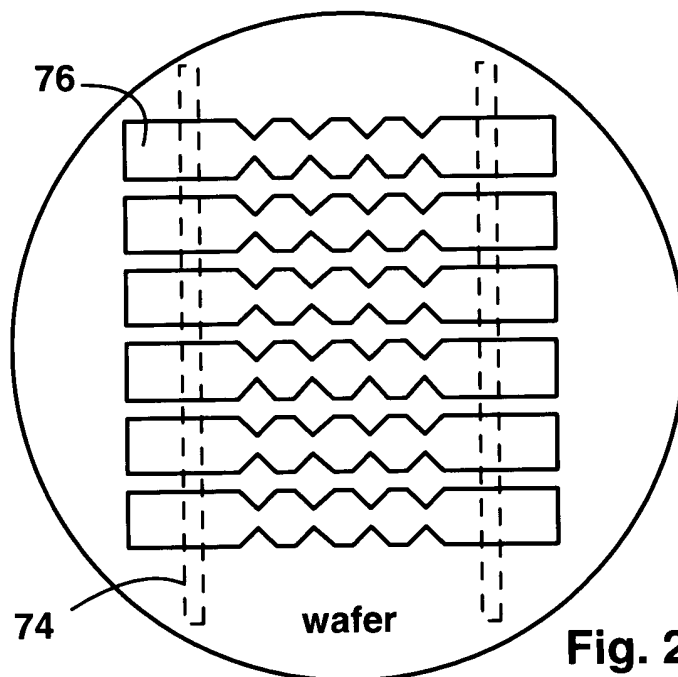


Fig. 20

00ET20"TOT5T960

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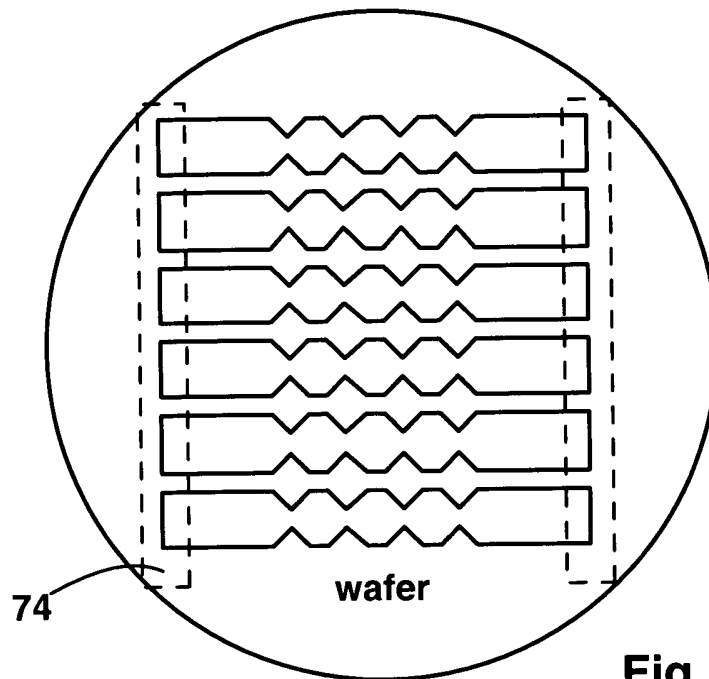


Fig. 21

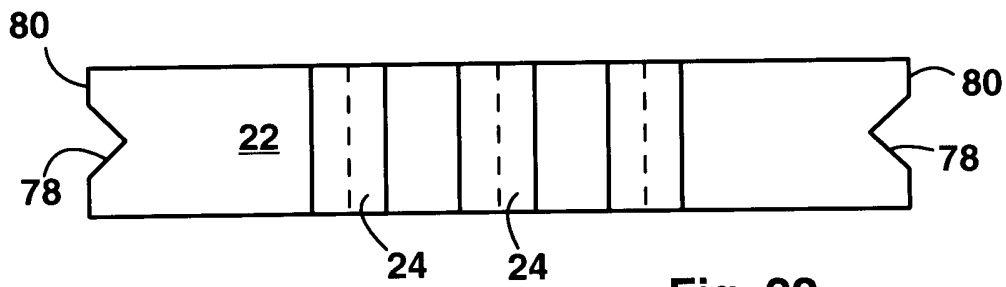
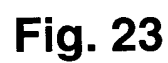


Fig. 22

00ET40" TOTST960



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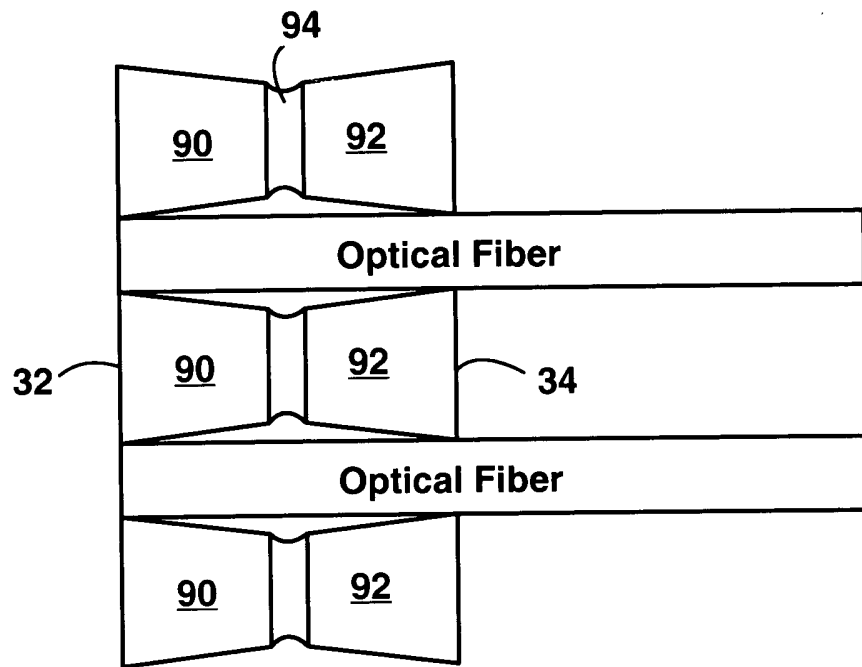


Fig. 26

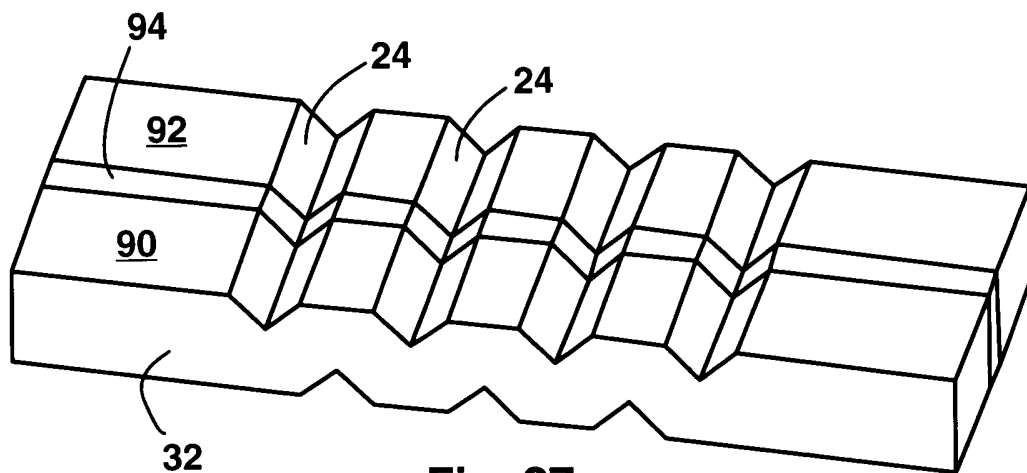


Fig. 27

09615101-031300

102



**silicon wafer**

**103**

**silicon wafer**

102



**silicon wafer**

**103**

**silicon wafer**

**104  
mask**

102



**silicon wafer**

**104  
mask**

